output of ALU 76a, and a data bus from read register bank 80. Also, an output bus from Bank A of general-purpose register 76b is connected to input mux A and an output bus from Bank B of general-purpose register 76b is connected to input mux B. All of the bus inputs to mux A and mux B are 32 bits wide. Control logic is provided to mux A and mux B to allow selection of individual 8-bit bytes of each operand transferred through to ALU 76a, as explained below in reference to local register instructions.--